IN THE CLAIMS

Please amend the claims as follows:

1 (Currently Amended). A data processor comprising:

a processor;

a first storage device; and

a second storage device connected between said processor and said first storage device,

wherein, when a predetermined data required by said processor does not exist in said second storage device, a plurality of data corresponding to one line of said second storage device, including said predetermined data, are read from said first storage device and transferred to a certain line of said second storage device by burst transfer, and

~~whereby~~ wherein, when an interrupt request occurs during said burst transfer, said burst transfer is suspended and an interrupt processing is started.

2 (Currently Amended). The data processor according to claim 1, wherein

said suspended burst transfer ~~suspended~~ is restarted after the completion of said interrupt processing.

3 (Currently Amended). The data processor according to claim 2, wherein

said suspended burst transfer ~~suspended~~ is restarted only when returning to the original program in which said burst transfer is suspended.

4 (Currently Amended). The data processor according to claim 2, wherein

when a plurality of interrupt requests occur, a plurality of interrupt processing are executed sequentially and, after the completion of the last interrupt processing, said suspended burst transfer ~~suspended~~ is restarted.

5 (Original). The data processor according to claim 2, further comprising:

an information register for keeping information about a point at which said burst transfer is suspended, wherein

among said plurality of data, only data not read from said first storage device due to suspension of said burst transfer are read from said first storage device and transferred based on said information when said burst transfer is restarted.

6 (Currently Amended). The data processor according to claim 2, wherein

said second storage device has a plurality of lines,

each line having information about a point at which said burst transfer is suspended, and

among said plurality of data, only data not read from said first storage device due to suspension of said burst transfer are read from said first storage device and transferred based on said information in said burst transfer restarted.

7 (Currently Amended). The data processor according to claim 1, wherein

said suspended burst transfer ~~suspended~~ is restarted when a certain line related to suspension of said burst transfer is accessed by said processor after said interrupt processing is completed.

8 (Currently Amended). The data processor according to claim 7, further comprising:

an information register for keeping information about a point at which said burst transfer is suspended, wherein

among said plurality of data, only data not read from said first storage device due to suspension of said burst transfer are read from said first storage device and transferred based on said information in said restarted burst transfer ~~restarted~~.

9 (Currently Amended). The data processor according to claim 7, wherein

said second storage device has a plurality of lines,

each line having information about a point at which said burst transfer is suspended, and

among said plurality of data, only data not read from said first storage device due to suspension of said burst transfer are read from said first storage device and transferred based on said information in said restarted burst transfer ~~restarted~~.

10 (Currently Amended). The data processor according to claim 1, wherein

said suspended burst transfer ~~suspended~~ is restarted when an instruction for terminating said interrupt processing is detected during execution of said interrupt processing.

11 (Currently Amended). The data processor according to claim 10, wherein

when a plurality of interrupt requests occur, a plurality of interrupt processing are executed sequentially and, when an instruction for terminating the last interrupt processing is detected, said burst transfer is restarted.

12 (Currently Amended). The data processor according to claim 10, further comprising:

an information register for keeping information about a point at which said burst transfer is suspended, wherein

among said plurality of data, only data not read from said first storage device due to suspension of said burst transfer are read from said first storage device and transferred based on said information in said restarted burst transfer ~~restarted~~.

13 (Currently Amended). The data processor according to claim 10, wherein

said second storage device has a plurality of lines,

each line having information about a point at which said burst transfer is suspended, and

among said plurality of data, only data not read from said first storage device due to suspension of said burst transfer are read from said first storage device and transferred based on said information in said restarted burst transfer ~~restarted~~.

14 (Original). The data processor according to claim 1, further comprising:

a register to which a predetermined priority related to an interrupt factor is set, and

a judgment unit comparing a priority of said interrupt request with said predetermined priority set in said register, and judging, from the comparison result, whether said burst transfer is suspended or not.

15 (Original). The data processor according to claim 1, further comprising:

a register to which permission or non-permission to suspend said burst transfer is set for each interrupt factor,

wherein said burst transfer is suspended only when said interrupt request has an interrupt factor that is set so as to permit suspension of said burst transfer.

16 (Currently Amended). The data processor according to claim 1, wherein

said interrupt ~~instruction~~ request is executed after executing an instruction that is already fetched before an interrupt instruction corresponding to said interrupt request is fetched.

17. (Currently Amended) The data processor according to claim 1, wherein

the processor processes instructions that are ~~processed~~ in a pipeline, the pipeline having an instruction fetch stage ~~fetching~~ that fetches the instructions, a decode stage ~~decoding~~ that decodes the instructions fetched by the instruction fetch stage, and an instruction execution stage ~~executing~~ that executes the instructions decoded by the ~~decoded~~ decode stage, wherein

the processor performs an interrupt process ~~is performed~~ when said interrupt request occurs, and

first and second processes are selectively performed by the processor, in accordance with a priority of said interrupt request, as the interrupt process,

said first process including a process that causes said instruction execution stage ~~executing~~ to execute an interrupt instruction corresponding to said interrupt request after executing an instruction that is already fetched before the interrupt instruction is fetched by the instruction fetch stage, and

said second process including a process that causes said instruction execution stage ~~executing~~ to execute the interrupt instruction before executing an instruction that is already fetched before the interrupt instruction is fetched by the instruction fetch stage and that is not yet executed by the instruction execution stage.

18 (Original). The data processor according to claim 17, further comprising:

a register to which a predetermined priority is set, and

a judgment unit comparing the priority of said interrupt request with the predetermined priority set in said register, and judging, from the comparison result, whether said first or second process is performed.

19 (Currently Amended). A data processor comprising:

a processor;

a first storage device; and

a second storage device connected between said processor and said first storage device,

wherein when a predetermined data required by said processor does not exist in said second storage device, a plurality of data corresponding to one line of said second storage device, including said predetermined data, are read from said first storage device and transferred to a certain line of said second storage device by burst transfer, and

when a first branch instruction is detected during a first burst transfer in the process of executing a first program, said first burst transfer is suspended and a second program, which is ~~as~~ a branch target program, is executed,

said data processor further comprising a register for keeping a first information about a point at which said first burst transfer is suspended, wherein

upon completion of execution of said second program, said first burst transfer suspended is restarted based on said first information.

20 (Currently Amended). The data processor according to claim 19, wherein,

when a second branch instruction is detected during a second burst transfer in the process of executing said second program, said second burst transfer is suspended and a third program, which is another ~~as a~~ branch target program, is executed,

said data processor further comprising another register for keeping a second information about a point at which said second burst transfer is suspended, wherein

upon completion of execution of said third program, said suspended second burst transfer ~~suspended~~ is restarted based on said second information.